WHAT IS CLAIMED IS:

1. A device for transforming a periodic input signal into an output signal of distinct frequency, comprising:

- two adjustable delay means receiving the input signal, the difference between the maximum and minimum delays of each delay means being greater than one period of the input signal;

- a multiplexer selecting the output signal of one or the other of the delay means;

- control means for, according to whether the frequency of the output signal must be smaller or greater than the frequency of the input signal, increasing or decreasing at the rate of the input signal, or at a multiple of this rate, the delay of the selected delay means, and controlling a minimum or maximum delay for the delay means which has not been selected, and

- a phase comparator adapted to changing the multiplexer selection when the transitions of the signals output by the delay means corresponding to a same transition of the input signal are offset by a duration greater than or equal to one period of the input signal.

2. The transformation device of claim 1, wherein the control means comprise means for setting the increase or decrease rate of the delay of the delay means.

3. The transformation device of claim 1, wherein the delay of the delay means varies by increments or decrements and the control means comprise means for setting the increment or decrement value.

4. The transformation device of claim 1, wherein each delay means comprises several delay elements in series, the output of each delay element being connected to the output of the delay means via a switch, the input of the first delay element being connected to the input of the delay means.

5. The transformation device of claim 1, wherein the phase comparator comprises two NAND gates with two inputs, the output of a NAND gate being connected to a first input of the other NAND gate, each NAND gate receiving on its second input one of the output signals of said delay means, one of these signals

being transmitted to the control input of a first flip-flop via a non-inverting circuit exhibiting a delay, the output of one of the NAND gates being connected to the data input of the first flip-flop, the output of the first flip-flop controlling a second flip-flop, having its output connected to its input via an inverter, the output of the second flip-flop controlling the multiplexer of the transformation device.

6. The transformation device of claim 1, wherein the delay of one of the delay means increases or decreases only during one or several cycles of a set of cycles of the input signal, the number of increases or decreases of the delay over a set of cycles being all the greater as the frequency of the output signal is remote from the frequency of the input signal.

7. A circuit, comprising:

an input node operable to receive a reference signal having a reference phase;

an output node;

a signal generator coupled to the input node and operable to generate from the reference signal a first signal having a first phase that varies from the reference phase during a first operational mode and a second signal having a second phase that varies from the reference phase during a second operational mode; and

a signal selector coupled to the signal generator and, in response to the first and second phases, operable to,

select the mode of operation,

couple the first signal to the output node during the first mode of operation, and

couple the second signal to the output node during the second mode of operation.

8. The circuit of claim 7 wherein the signal generator:

increases a difference between the first and reference phases and maintains constant a difference between the second and reference phases during the first operational mode; and

increases the difference between the second and reference phases and maintains constant the difference between the first and second reference phases during the second operational mode.

9. The method of claim 7 wherein:

during the first operational mode the signal generator varies the difference between the first and reference phases at least once per cycle of the reference signal; and

during the second operational mode the signal generator varies the difference between the second and reference phases at least once per cycle of the reference signal.

10. The method of claim 7 wherein:

during the first operational mode the signal generator varies the difference between the first and reference phases at least once but less than once per cycle of the reference signal; and

during the second operational mode the signal generator varies the difference between the second and reference phases at least once but less than once per cycle of the reference signal.

11. The circuit of claim 7 wherein:

the signal generator is operable to,

generate first edges of the first signal in response to corresponding reference edges of the reference signal, and

generate second edges of the second signal in response to the corresponding reference edges of the reference signal; and

the signal selector is operable to,

select the first operational mode when the first edges of the first signal lag the second edges of the second signal by less than one cycle of the reference signal, and

select the second operational mode when the second edges of the second signal lag the first edges of the first signal by less than one cycle of the reference signal.

12. An integrated circuit, comprising:

a clock generator operable to generate a clock signal, the clock generator comprising,

an input node operable to receive a reference signal having a reference phase,

an output node,

a signal generator coupled to the input node and operable to generate from the reference signal a first signal having a first phase that varies from the reference phase during a first operational mode and a second signal having a second phase that varies from the reference phase during a second operational mode, and

a signal selector coupled to the signal generator and, in response to the first and second phases, operable to,

select the mode of operation,

couple the first signal to the output node as the clock signal during the first mode of operation, and

couple the second signal to the output node as the clock signal during the second mode of operation.

13. The integrated circuit of claim 12, further comprising a transmitter coupled to the clock generator and operable to transmit data in synchronization with the clock signal.

14. An electronic system, comprising:

an integrated circuit, comprising,

a clock generator operable to generate a clock signal, the clock generator comprising,

an input node operable to receive a reference signal having a reference phase,

an output node,

a signal generator coupled to the input node and operable to generate from the reference signal a first signal having a first phase that varies from the reference phase during a first operational mode and a second signal having a second phase that varies from the reference phase during a second operational mode, and

a signal selector coupled to the signal generator and, in response to the first and second phases, operable to,

select the mode of operation,

couple the first signal to the output node as the clock signal during the first mode of operation, and

couple the second signal to the output node as the clock signal during the second mode of operation.

15. The electronic system of claim 14 wherein the integrated circuit comprises a transmitter that is operable to clock transmitted data with the clock signal.

16. A method, comprising:

varying a phase of a first signal relative to a phase of a reference signal; and

varying a phase of a second signal relative to the phase of the reference signal when the phase of the second signal has a predetermined relationship to the phase of the first signal.

17. The method of claim 16 wherein:

varying the phase of the first signal relative to the phase of the reference signal comprises incrementing the phase of the first signal relative to the phase of the second signal; and

varying the phase of the second signal relative to the phase of the reference signal comprises incrementing the phase of the second signal relative to the phase of the second signal.

18. The method of claim 16 wherein varying the phase of the second signal relative to the phase of the reference signal comprises varying the phase of the second signal when a difference between the phases of the first and second signals transitions from being less than one period of the second signal to being equal to or greater than one period of the second signal.

19. The method of claim 16 wherein varying the phase of the second signal relative to the phase of the reference signal comprises varying the phase of the second signal when a difference between the phases of the first and second signals transitions from being less than one period of the reference signal to being equal to or greater than one period of the reference signal.

20. A method for generating a clock signal, comprising:

generating first and second signals having respective first and second phases from a reference signal having a reference phase;

generating the clock signal equal to the first signal and increasing a difference between the first and reference phases during a first mode when the first signal lags the second signal by less than one cycle of the reference signal; and

generating the clock signal equal to the second signal and increasing a difference between the second and reference phases during a second mode when the second signal lags the first signal by less than one cycle of the reference signal.

21. The method of claim 20, further comprising:

maintaining a substantially constant difference between the second and reference phases during the first mode; and

maintaining a substantially constant difference between the first and reference phases during the second mode.

22. The method of claim 20 wherein:

increasing the difference between the first and reference phases comprises increasing a delay between the first and reference signals by a predetermined amount each cycle of the reference signal during the first mode; and

increasing the difference between the second and reference phases comprises increasing a delay between the second and reference signals by the predetermined amount each cycle of the reference signal during the second mode.

23. The method of claim 20 wherein:

increasing the difference between the first and reference phases comprises increasing a delay between the first and reference signals by a predetermined amount at least once during the first mode; and

increasing the difference between the second and reference phases comprises increasing a delay between the second and reference signals by the predetermined amount at least once during the second mode.